II. Amendment to the Claims

Claims 1-30 are pending in the present application. Claims 1-11, 13, 15-19, 21 and 27 have been canceled. Claims 12, 14, 20, 22, 23, 25, 26, 28 and 29 have been amended as set forth below. New Claim 31 has been added. This listing and version of the claims replaces all prior listings and version of the claims.

1-11. (canceled)

12. (currently amended) A semiconductor memory device, comprising:

~~a bit line;~~

~~a plurality of memory cells and a bit switch coupled between said memory cells and a supply voltage node;~~

~~means for detecting a bit line current provided to said memory cells; and~~

<u>a plurality of bit lines coupled to a supply voltage node, each of said bit lines comprising respective plurality of memory cells coupled to said supply voltage node through a respective bit switch, wherein a group of said memory cells are addressable together for programming or overerase correction;</u>

means for adjusting a supply voltage at said supply voltage node responsive to <u>a detection of a total bit line current provided to said plurality of bit lines</u> ~~said detected bit line current~~ to at least partially compensate for a voltage drop across said bit switch<u>es</u>, said voltage drop being dependent at least in part on said <u>total</u> bit line current<u>, said adjustment comprising increasing said supply voltage responsive to a detected increase in said total bit line current and decreasing said supply voltage responsive to a detected decrease in said total bit line current, wherein said adjusting means comprises:</u>

a differential amplifier having an output coupled to said supply voltage node; and

a reference voltage generating circuit having an output coupled to a reference voltage input of said differential amplifier, said reference voltage generating circuit comprising a resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

13. (canceled)

14. (amended) The semiconductor device of claim 12, wherein said ~~further comprising means for~~ adjusting means ~~said supply voltage to~~ maintains a bit line voltage at a ~~said~~ memory cell from said plurality of memory cells that is substantially constant during programming or overerase correction ~~of said cell~~.

15-19. (canceled)

20. (currently amended) A ~~The~~ semiconductor memory device, comprising: ~~of claim 15,~~

a plurality of bit lines coupled to a supply voltage node, each of said bit lines comprising respective plurality of memory cells coupled to said supply voltage node through a respective bit switch, wherein a group of said memory cells are addressable together for programming or overerase correction;

means for detecting a total bit line current provided to said plurality of bit lines;

means for adjusting said supply voltage responsive to said detected total bit line current to at least partially compensate for a voltage drop across said bit switches, said voltage drop being dependent at least in part on said total bit line current,

wherein said supply voltage comprises a fixed reference voltage component and variable voltage component responsive to said detected total bit line current,

said semiconductor device further comprising means for incrementally adjusting a relationship between said variable component and said total bit line current in response to respective memory cells from said group of memory cells reaching a programmed state,

wherein said adjusting means comprises a reference voltage generating circuit comprising a tunable resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

21. (canceled)

22. (currently amended) The semiconductor device of claim 20 ~~21~~, further comprising means for adjusting a resistance of said tunable resistance circuit responsive to a plurality of control signals indicative of whether each of said respective cells from said group of memory cells is in a programmed state.

23 (currently amended) The semiconductor device of claim 22, wherein said relationship ~~amount~~ is adjusted after each respective cell from said group of memory cells reaches said programmed state.

24. (original) The semiconductor device of claim 20, further comprising means for generating said variable voltage component.

25. (currently amended) The semiconductor memory device of claim 12 ~~15~~, wherein said semiconductor memory device is a flash memory device comprising flash memory cells organized in an array of I/O blocks, each I/O block comprising a plurality of columns and plurality of rows, said array of I/O blocks comprising said plurality of bit lines.

26. (currently amended) A semiconductor memory device comprising flash memory cells organized in an array comprising a plurality of columns and plurality of rows, said plurality

of columns comprising a plurality of bit lines each comprising a respective one of the memory cells coupled to a supply voltage through a respective bit switch, wherein a group of said memory cells are addressable together for programming, said semiconductor device further comprising:

means for detecting a total bit line current provided to a plurality of bit lines associated with said group of memory cells;

a regulated supply voltage source for providing said supply voltage, said supply voltage comprising a fixed reference voltage component and a variable voltage component responsive to said detected total bit line current, wherein said supply voltage is adjusted to track changes in total bit line current provided to said plurality of bit lines associated with said group; and

means for adjusting, in response to respective memory cells reaching a programmed state, a relationship between said variable voltage component and said total bit line current, said adjusting means comprising a reference voltage generating circuit comprising a tunable resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

27. (canceled)

28. (currently amended) The semiconductor device of claim 26 ~~27~~, further comprising means for adjusting a resistance of said tunable resistance circuit responsive to a control signal indicative of whether each of said respective cells are in a programmed state.

29 (currently amended) The semiconductor device of claim 28, wherein said relationship ~~amount~~ is adjusted after each respective cell reaches said programmed state.

30. (original) A semiconductor memory device, comprising:

a bit line;

a memory cell and a bit switch coupled between said memory cell and a supply voltage node;

a current mirror circuit configured to mirror a bit line current through said memory cell with a reduction ratio;

a voltage source having an output coupled to said supply voltage node and responsive to a reference voltage; and

a reference voltage generator circuit having an output coupled to a reference voltage input of said voltage source, said reference voltage generator circuit comprising a resistance circuit coupled to said current mirror circuit,

wherein said reference voltage generator circuit provides a reference voltage for said voltage source that is responsive to said mirrored bit line current,

whereby said supply voltage at said supply voltage node is adjusted responsive to said bit line current to at least partially compensate for a voltage drop across said bit switch, said voltage drop being dependent at least in part on said bit line current.

31. (new) The semiconductor memory device of claim 20, wherein said semiconductor memory device is a flash memory device comprising flash memory cells organized in an array of I/O blocks, each I/O block comprising a plurality of columns and plurality of rows, said array of I/O blocks comprising said plurality of bit lines.

III. Amendments to the Specification

Please amend Paragraph 29 as follows:

[0029] As noted above, the bit switch path can be turned off for a programmed cell or I/O by signal PD[n] coupled to the control gate of PMOS QPL. Each signal PD is the inverse state of the respective signal PDN and its logical high is set to VDQ2 and logical low to VSS.

Please amend Paragraph 30 as follows:

[0030] The memory circuit of FIG. 5, although not shown, may still include a leakage path from node VDQ2 to ground as shown in FIG. 2 to reduce any initial overshoot of VDQ2 discussed above in connection with FIG. 2. This current, however, will be mirrored in circuit 200 by the ~~cell~~ bit line current detector PMOS QP1. The effect of this leakage current can be neutralized by turning on the leakage current circuit for a time interval, for example, 1 μs, to stabilize the VDQ2 level and turning off the leakage current circuit thereafter. A timing circuit (not shown) may be used to control this time duration. The timer that generates control signals for the timing of program pulses, overerase pulses and erase pulses may be used. During this interval, the input to the differential amplifier 122 can be set to VR rather than VRP, essentially disconnecting Detector and Tuner Circuit 200 from differential amplifier 122 and setting VDQ2 to a constant voltage. After this time interval, VRP is connected to the differential amplifier and, optionally, a small leakage path circuit can be turned on to replace the original leakage path circuit for avoiding VDQ2 overshoot. The leakage path circuit may comprise, as one of ordinary skill familiar with the prior art circuit of FIG. 2 will recognize, one or more NMOS transistors coupled in series to node VDQ2. If the voltage at VDQ2 is too high, the current will sink through the NMOS transistors to ground. Once the VDQ2 level is stabilized, the leakage current can be reduced by connecting smaller NMOS transistors to node VDQ2.

Please amend Paragraph 33 as follows:

[0033] Tables 2-1 and 2-2 below illustrate the results of a software simulation of the circuit of FIG. 6, with resistors used to simulate the bit switch resistances. The tables illustrate two conditions – (1) there is only one erased cell to be programmed, or one bit line to be overerase corrected, and (2) there are eight erased cells to be programmed or eight bit lines to be overerase corrected. Tables 2-1 and 2-2 illustrate that the VBL difference when total bit line current is increased is reduced by the change in VRP, and thus VDQ2, as the total bit line current is increased or decreased. The simulation illustrates that the change in VBL due to changes in bit line current is less than or equal to about 0.17 volts for each simulation. The simulation assumed that the temperature coefficient of resistance of Rt is 1000 ppm/°C ~~ppm/0°C~~. The "VBL" voltage in the chart shows the bit line voltage on a bit line with non-zero bit line current (i.e., on a bit line being programmed or overerase corrected) and for the bit line with zero bit line current and QPL "on".[[.]] The VBL voltage will be VDQ2 for the bit line with zero bit line current and QPL "on".

Please amend Paragraph 34 as follows:

[0034] Tables 3-1 and 3-2 below illustrate the results of a software simulation of the circuit of FIG. 6, only using transistors to simulate the bit switch resistances. The tables illustrate two conditions – (1) there is only one erased cell to be programmed, or one bit line to be overerase corrected, and (2) there are eight erased cells to be programmed or eight bit lines to be overerase corrected. Tables 3-1 and 3-2 indicate results that are similar to Tables 2-1 and 2-2 in that VBL stays relatively constant (i.e., the largest change in VBL due to a change in total bit line current was only about 0.2V). The simulation assumed that the temperature coefficient of resistance of Rt is 1000 ppm/°C ~~ppm/0°C~~.